Amendments to the Drawings:

The attached sheet of drawings includes changes to Figure 2. This sheet replaces the original sheet including Figure 2. In Figure 2, structures 32, 34 and 35 have been related to structure 2 in Figure 1. Also, structures 30, 31, and 32 have been related to structure 3 in Figure 1.

Attachments: Replacement Sheet
Annotated Sheet Showing Changes

REMARKS

A. GENERALLY

Claims 1-11 remain in the Application. Claims 1 and 2 have been amended. No new matter has been added.

B. CLAIM REJECTIONS

1. Claim Rejections Pursuant to 35 U.S.C. § 102

Claims 1-4 and 6-8 have been rejected under 35 U.S.C. 102(b) as being anticipated by European Patent Application Publication EP 0875882 filed by Schiefer et al. (hereinafter, "Schiefer").

Claim 1 (as amended) recites the following limitations:

1. (Currently Amended) A display method comprising:

generating images comprising source data and source frame synchronization instants having a source frame rate,

storing the source data in a frame memory under control of a first address pointer having a start address being determined by the source frame synchronization instants,

reading during a read period display data from the memory under control of a second address pointer having a start address being determined by display frame synchronization instants having a display frame rate,

displaying the display data on a matrix display, and

controlling the source frame rate or the display frame rate to obtain, in a stable situation, the first address pointer and the second address pointer starting with an offset in time which has a fixed polarity during the read period and a ratio of two between the display frame rate and the source frame rate.

The Office Action asserts that these limitations are met by Schiefer.

Schiefer describes a video format converter that comprises a display timing controller. The display timing controller operates in a free-running mode in which the display output is not synchronized to the input signal and in a frame lock mode in which the input video source clock is "locked" to the display clock.

The lock mode utilizes a lock event generator that determines a synchronizing event from a pre-determined point in a video frame (determined by horizontal and vertical time pulse counts). When a synchronizing event occurs, a lock event pulse forces synchronization of the display timing generator with video input signal according to a selected operating mode of the display synchronizer.

The Office Action asserts that the limitation, "controlling the source frame rate or the display frame rate to obtain...the first address pointer and the second address pointer starting with an offset in time which has a fixed polarity during the read period" is met by Schiefer, Col. 17, line 12-20:

> The lock event is a single pulse which occurs once per video input frame which can then be used to synchronize the display output frame rate to the input frame rate.
>
> Since interlaced formats use a ½ line offset between the input odd or even fields, in order to achieve interleaving of the active lines to produce complete frames, then an obvious adaptation of the above-described lock event controller is to add the ability to generate a lock event once per field during interlaced video input. To do this every other field would have the lock event delayed by ½ of an input line period in order to maintain a constant period between lock events.

Schiefer describes synchronizing the output frame rate to the input frame rate but does not teach or reasonably suggest obtaining the first address pointer (the write pointer) and the second address pointer (the read pointer) with an offset in time. Schiefer also describes imposing a delay in the lock events of interlaced formats so as to generate lock events once per field having a constant period between lock events. In either case, the lock event is used to activate the display clock at a pre-determined point in the reading of a frame but does not establish an offset in time having a fixed polarity for obtaining the first and second address pointers.

The Office Action further asserts that the limitation, "controlling the source frame rate or the display frame rate to obtain... the first address pointer and the second address pointer ... and a ratio of two between the display frame rate and the source frame rate," is met by Schiefer, Col. 21, lines 15-20:

> Therefore, the LINE SYNC MODE provides a means for producing a display line rate that is controlled as a fractional multiple of the input video main clock resulting in a display line rate that follows any variations in the input video main clock and therefore follows any variation in the input video line rate.

Schiefer describes a display synchronizer **410** that supports four fundamental operating modes -- free run mode, clock synchronized mode, frame synchronized mode and line synchronized mode. (See, Schiefer, Col. 18, line 3 through Col. 23, line 4.) The display synchronizer is programmable to select one of these modes. The selected mode determines the method for synchronizing the display timing generator **430** with the input video source. When the free run mode is active, there is no synchronization of display video timing with the input video timing by means of the display synchronizer **410**. The clock synchronized mode provides a means for forcing the display video timing to synchronize to a lock event in the input video

timing initially on start up but allows the display video timing to free run once started. Again, in this mode, Schiefer does not teach the limitation, "controlling the source frame rate or the display frame rate to obtain... the first address pointer and the second address pointer ... and a ratio of two between the display frame rate and the source frame rate."

The line synchronized mode forces the display video timing to synchronize to a lock event on a frame by frame basis. The lock event is not, however, described as controlling the source frame rate or the display frame rate to obtain... the first address pointer and the second address pointer ... and a ratio of two between the display frame rate and the source frame rate. Further, Schiefer does not describe how the video format converter could perform such a limitation.

The frame synchronization mode forces the display video timing to synchronize to a lock event on a frame by frame basis. The lock event is not, however, described as controlling the source frame rate or the display frame rate to obtain... the first address pointer and the second address pointer ... and a ratio of two between the display frame rate and the source frame rate. Further, Schiefer does not describe how the video format converter could perform such a limitation.

Schiefer does not describe that the source frame rate or the display frame rate is independently controllable as recited in claim 1. Based on the foregoing, claim 1 (as amended) is not anticipated by Schiefer.

Claim 2 (as amended) recites limitations similar in scope to those discussed in the context of claim 1 (as amended). For the reasons set forth above, claim 2 (as amended) is not anticipated by Schiefer.

Claims 3-4 and 6-8 depend directly or indirectly from claim 2 (as amended) and recite all of the limitations of that base claim. For the reasons set forth above, claims 3-4 and 6-8 recite limitations not taught or reasonably suggested by Schiefer and are not anticipated by that reference.

2. **Claim Rejections Pursuant to 35 U.S.C. § 103**

Claim 5 has been rejected under 35 U.S.C. 103(b) as being unpatentable over Schiefer.

Claim 5 recites the limitation, "wherein the means for adapting are arranged to obtain the offset in time between the first pointer and the second pointer being substantially equal to half a source write period, the source write period being the period in time required for the storing of the source data of one source frame of the source data."

The Office Action provides a list of benefits of providing the means described in the limitation but does not cite Schiefer or any other reference to support the conclusion that the claim is obvious. Applicant respectfully submits that the Office Action has failed to establish a prima facie case of obviousness with respect to claim 5.

Additionally, claim 5 depends indirectly from claim 2 (as amended). As previously demonstrated, claim 2 (as amended) recites limitations not taught or reasonably suggested by Schiefer. For these reasons, claim 5 is patentable over Schiefer.

Claims 9-11 have been rejected under 35 U.S.C. 103(b) as being unpatentable over Shiefer as applied to claims 1-8 in further view of U.S. Patent Application 2003/0164897 filed by Chen, et al. (hereinafter, "Chen").

Claims 9-11 depend from claim 2 (as amended). As previously demonstrated, claim 2 (as amended) recites limitations not taught or reasonably suggested by Schiefer. The Office Action does not assert that Chen teaches these limitations. Based on the foregoing and the arguments presented with respect to claim 2 (as amended), claims 9-11 are patentable over Schiefer and Chen.

C. CONCLUSION

Applicant respectfully submits that the claims as currently listed are in condition for allowance. Applicant requests that this response be entered and that the current rejection of the claims now pending in this application be withdrawn in view of the above amendments, remarks and arguments.

Respectfully submitted,

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ATTACHMENTS:

1. Replacement Sheet for Figure 2
2. Annotated Sheet Showing Changes in Figure 2

ATTACHMENT 1

Replacement Sheet for Figure 2